**Amendments to the Claims:**

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1.(Currently Amended) A digital signal processing apparatus for executing a plurality of operations included in a loop, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, and control means for controlling said functional units, characterized in that said control means comprises a fetch unit, a decode unit, and a plurality of control units responsive to said decode unit, wherein each functional unit has a private control unit for controlling function of ~~an associated~~the each functional unit, including controlling a number of repetitions of execution of the function, and each functional unit is adapted to execute operations in an autonomous manner under control of the private control unit associated therewith so that access to an external instruction memory is reduced, including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction, wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations, and a counter indicating how often the one operation or the sequence of operations still has to be executed.

2.(Previously Presented) An apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units.

3.(Previously Presented) A digital signal processing apparatus for executing a plurality of operations included in a loop, comprising a plurality of functional units

wherein each functional unit is adapted to execute operations, and respective private control means for said each functional unit for controlling said functional units in coordination with one another in response to a single fetch unit and a single decode unit, characterized by FIFO ( first-in/first-out) register means adapted for supporting data-flow communication among said functional units, wherein said functional units transfer control to the single fetch unit upon completion of an operation included in the loop and execute instructions of a subsequent loop instead of being stalled or executing a no-operation instruction, each functional unit being adapted to execute a set of operations in an autonomous manner under control of its respective private control means associated therewith so that access to an external instruction memory is reduced, wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations, and a counter indicating how often the one operation or the sequence of operations still has to be executed.

Claim 4 (Canceled)

5.(Previously Presented) An apparatus according to claim 2, characterized in that said FIFO register means comprises a plurality of FIFO registers.

6.(Previously Presented) An apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit.

7.(Previously Presented) An apparatus according to claim 1, which apparatus is adapted to execute a pipeline consisting of a plurality of stages, wherein each stage comprises a functional unit.

8.(Previously Presented) An apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, wherein said

counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit.

9.(Previously Presented) An apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units.

10.(Previously Presented) A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units wherein each functional unit is adapted to execute operations included in a loop, characterized in that said functional units are controlled by control means including a single fetch unit, a single decode unit and a plurality of private control units wherein at least one private control unit is operatively associated with a respective functional unit so that each functional unit is able to execute operations in an autonomous manner under control of the private control unit associated therewith so that access to an external instruction memory is reduced, including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction, the control unit controlling a number or repetitions of execution of its associated functional unit, wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations, a counter indicating how often the one operation or the sequence of operations still has to be executed.

11.(Previously Presented) An apparatus according to claim 9, characterized in that data-flow communication among said functional units is supported by FIFO (first-in/first-out) register means.

Claim 12 (Canceled)

13.(Previously Presented) An apparatus according to claim 11, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by at least one of said functional units.

14.(Previously Presented) An apparatus according to claim 1, characterized in that the number of times an instruction stored has to be executed by at least one of said functional units is counted by the corresponding control unit.

Claim 15 (Canceled)